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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,204	09/24/2003	Jeffrey L. Wise	IS01388MCG	6946

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EXAMINER	
PASIA, REDENTOR M	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,204	WISE ET AL.	
	Examiner	Art Unit	
	Redentor M. Pasia	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-11,13-15,17-25 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-11, 13-15, 17-25, and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment filed on October 17, 2007 has been entered. Claims 1, 4, 5, 9, 11, 13-15, 17, 23, 25, and 27-29 have been amended. Claims 6, 12, 16, 26 and 30 have been canceled. No claims have been added. Claims 1-5, 7-11, 13-15, 17-25, and 27-29 are still pending in this application, with claims 1, 9, 13, 17, 23, and 27 being independent.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.

1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1, 5-12, and 23-26 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims1-2, 5-9, 14-17 and 19-21 of copending Application No. 10/671203. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

As to claim 1 of the application, claim 2 (dependent to claim 1) of the co-pending application shows a link receiver providing a plurality of data credits to a link transmitter (claim 1); the link transmitter transmitting a packet to the link receiver on an ingress link (claim1); the link receiver storing the packet in a plurality of receiver buffers (claim 1); the link receiver transmitting the packet out of the plurality of receiver buffers on a

egress link (claim 2 dependent on claim 1); placing the plurality of receiver buffers into a free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the free buffer pool corresponds to additional data credits (claim 2 dependent on claim 1); and the link receiver transmitting a flow control packet to the link transmitter, wherein the flow control packet comprises the additional data credits (claim 1). However, claim 2 (dependent on claim 1) does not explicitly show a step of diminishing the plurality of data credits as the packet is transmitted. Claim 1 of the co-pending application shows the step of link receiver updating the free buffer pool. It is obvious to one of ordinary skill in the art at the time of the invention that updating the free buffer pool means that either there is additional space in the free buffer pool (when packet is transmitted out of the receive buffers onto the network) or less space in the buffer pool (when packet enter the receive buffers).

As to claim 5 of the application, claim 5 (in view of claim 1 and 2) of the co-pending application shows the link transmitter has a plurality of logical channels, and wherein the link transmitter selects to which of the plurality of logical channels to allocate the additional data credits.

As to claim 6 of the application, claim 6 (in view of claim 1 and 2) of the co-pending application shows the link transmitter has a plurality of logical channels, and wherein the link receiver selects to which of the plurality of logical channels to allocate the additional data credits.

As to claim 7 of the application, claim 7 (in view of claim 1 and 2) of the co-pending application shows the link transmitter and the link receiver operate in a switch fabric network

As to claim 8 of the application, claim 8 (in view of claim 1 and 2) of the co-pending application shows the switch fabric network is one of an Infiniband network and a Serial RapidIO network.

As to claim 9 of the application, refer to claim 1 rejection.

As to claim 10 of the application, claim 4 (in view of claim 1 and 2) of the co-pending application shows the packet begins transmitting out of the plurality of receiver buffers when one of the plurality of receiver buffers is empty.

As to claim 11 of the application, refer to claim 5 rejection.

As to claim 12 of the application, refer to claim 6 rejection.

As to claim 23 of the application, claim 17 (dependent from claim 16) of the co-pending application, shows a computer-readable medium containing computer instructions for instructing a processor to perform a method of early buffer return, the instructions comprising: a link transmitter transmitting a packet to a link receiver on an

ingress link (claim 16); the link receiver storing the packet in a plurality of receiver buffers claim 16); the link receiver transmitting the packet out of the plurality of receiver buffers on a egress link (claim 17 dependent from claim 16); and placing the plurality of receiver buffers into a free buffer pool when the packet begins transmitting out of the plurality of receiver buffers, wherein the free buffer pool corresponds to additional data credits (claim 17 dependent from claim 16). However, claim 17 (dependent on claim 16) does not explicitly show a step of diminishing the plurality of data credits as the packet is transmitted. Claim 23 of the co-pending application shows the step of link receiver updating the free buffer pool. It is obvious to one of ordinary skill in the art at the time of the invention that updating the free buffer pool means that either there is additional space in the free buffer pool (when packet is transmitted out of the receive buffers onto the network) or less space in the buffer pool (when packet enter the receive buffers).

As to claim 24 of the application, claim 19 of co-pending application shows the packet begins transmitting out of the plurality of receiver buffers when one of the plurality of receiver buffers is empty.

As to claim 25 of the application, claim 19 of co-pending application shows the link transmitter has a plurality of logical channels, and wherein the link transmitter selects to which of the plurality of logical channels to allocate the additional data credits.

As to claim 26 of the application, claim 19 of co-pending application shows the link transmitter has a plurality of logical channels, and wherein the link receiver selects to which of the plurality of logical channels to allocate the additional data credits.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-11, 13-15, 17-25, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bloch et al. (US 6,922,408 B2; hereinafter Bloch) in view of Jones et al. (US 6944173 B1; hereinafter Jones) in further view of Takase et al. (US 7023799 B2; hereinafter Takase)

As to claims 1, and 9, Bloch shows a method comprising: providing from a link receiver, a plurality of data credits to a link transmitter (col. 7, lines 18-21; shows that

the receiver updates the available credits and when possible, provides additional credits to the transmitter.); transmitting a packet from the link transmitter to the link receiver on an ingress link (col. 4, lines 58-63; shows switch 20 in a packet switching fabric. The packet switching fabric comprises an Infiniband (IB) fabric. At col. 1, lines 38-40, it shows that the switch port at each end of each physical link includes a transmitter and a receiver for sending packets to and receiving packets from the corresponding port at the other end of the link.); diminishing the plurality of data credits (at the link transmitter – as to claim 9) as the packet is transmitted (Figure 4; col. 7, lines 15-23; shows a response of the receiver (port 24) to data packet received from transmitter (entity 27) wherein the response involves a process by which the receiver updates the available credits and when possible, provides additional credits to the transmitter. The process takes place whenever port 24 receives a new packet. Also at col. 1, lines 40-45, Bloch shows that the receiver provides the transmitter with credit limits indicating the total amount of data that the transmitter has been authorized to send. The transmitter is not permitted to send anymore data if the credit limit has been exhausted (diminished).); storing the packet in a receiver buffer at the link receiver (col. 3, lines 27-29; shows a step of receiving the data in the receive buffer responsive to the allocated credits.); transmitting the packet out of the receiver buffer at the link receiver on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission through the network. At col. 8, lines 13-21, Figure 1; shows the method (figure 5 flowchart) is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward transmission.); placing the plurality of receiver buffers into

a free buffer pool as the packet is transmitting out of the plurality of receiver buffers, wherein the free buffer pool corresponds to additional data credits (Based from the specification of the application (Wise) at Par. 0033, it shows that free buffer pool represents the empty portion of the receiver buffer. Therefore, the examiner interprets this limitation as resetting the receive buffer space that was used by the packet back to being an empty/unused part of the receive buffer. This interpretation is also applied to the remainder of the office action. Bloch shows at Figure 5, a flow chart that illustrates a method of reallocation of credits in receive queues 28 after a data packet has passed out of buffer 25. At col. 8, lines 22- 51, shows the different scenarios of credit (of buffer space) reallocation when the packet was passed out of the buffer.); and transmitting a flow control packet from a link receiver to the link transmitter, wherein the flow control packet comprises the additional data credits (col. 1, lines 43-47; show that the transmitter receives a flow control packet from the receiver indicating that additional credit is available.). However, Bloch does not show the step of allocating at the link transmitter the plurality of data credits to a plurality of logical channels and does not show a plurality of receiver buffers.

Jones shows the step of allocating at the link transmitter the plurality of data credits to a plurality of logical channels (Figure 1, plurality of virtual channels, VC0-N; Figure 5; col. 2, lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify method of Bloch to include the selection of logical channels of Jones in order to bypass the need for an acknowledgement packet,

resulting in reliable transmissions and efficient use of bandwidth (Jones, col. 2, lines 7-9). Jones does not show a plurality of receiver buffers.

Takase shows a plurality of packet buffers (Figure 2, Packet Buffer 20-1 to 20-n). It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method of modified Bloch to include the plurality of packet buffers of Takase, as shown above, in order to increase the amount of data to be transmitted and/or received in a device.

As to claim 2, further modified Bloch shows that the ingress link has an ingress link speed, and the egress link has an egress link speed (Takase: Figure 11; input line has a rate of 1Gbps and output line has a rate of 2.4 Gbps.), wherein placing the plurality of receiver buffers into the free buffer pool comprises: if the egress link speed is less than the ingress link speed, placing the plurality of receiver buffers in the free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers (Takase: Figure 6C, col. 8, lines 15-19; shows that the input rate flows at a rate over the minimum guaranteed bandwidth (output rate). At col. 8, lines 1-14; Figure 6C, Takase shows that as long as the level of the leaky bucket repeatedly increases and decreases around the threshold as the lower limit, and the input packets are transferred to the output line without causing excessive residence in the packet buffer.), and wherein the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed (Takase: col. 8, lines 1-3; shows that to the leaky bucket each time a packet is read out from the buffer (output queue), "water" of a volume proportional to the

packet length is poured. The leaky bucket shown in Figures 6A-6E, shows the relationship between the input speed and the output place.); and if the egress link speed is one of greater than and equal to the ingress link speed, placing the plurality of receiver buffers into the free buffer pool when the packet begins transmitting out of the plurality of receiver buffers (Figures 6D-6F; col. 8, lines 27-33; shows that when the level largely drops below the threshold (input rate < output rate), the transmission right is frequently granted to the packet buffer corresponding to the leaky bucket).

As to claims 3 and 10, further modified Bloch shows that the packet begins transmitting out of the plurality of receiver buffers when one of the plurality of receiver buffers is empty (Takase: col. 8, lines 34-46, that when the level drops largely below the threshold, and after that, packets flow in a rate over the minimum guaranteed bandwidth of 600 Mbps, during a period until the level reaches the threshold TH600, packets are transmitted to the output line at a rate over the minimum guaranteed bandwidth. A level that is largely below the threshold also covers the lowest level possible (an empty buffer).).

As to claim 4, further modified Bloch shows that the portion of the packet is equal to one minus the ratio of the egress link speed to the ingress link speed (Takase: col. 8, lines 1-19 and Figure 6C, shows that to the leaky bucket, each time a packet is read out from the packet buffer (output queue), "water" of a volume proportional to the packet length is poured. In the case where packets flow in at a rate over the minimum

guaranteed bandwidth of 600 Mbps from the input line, if the packets flow output from the packet buffer is controlled to 600 Mbps, the amount of packets residual in the packet queue increases.).

As to claim 5 and 11, further modified Bloch shows the step of selecting from the plurality of logical channels to allocate the additional data credits at the link transmitter (Jones: Figures 1 and 5; col. 2, lines 13-21).

As to claim 7, further modified Bloch shows that the link transmitter and the link receiver operate in a switch fabric network (Bloch: col. 4, lines 58-63).

As to claim 8, further modified Bloch shows that the switch fabric network is one of an Infiniband network (col. 4, lines 58-63).

As to claim 13, Bloch shows a method, comprising: transmitting a packet from the link transmitter to a link receiver on an ingress link (col. 4, lines 58-63; shows switch 20 in a packet switching fabric. The packet switching fabric comprises an Infiniband (IB) fabric. At col. 1, lines 38-40, it shows that the switch port at each end of each physical link includes a transmitter and a receiver for sending packets to and receiving packets from the corresponding port at the other end of the link.); diminishing the plurality of data credits at the link transmitter as as the packet is transmitted (Figure 4; col. 7, lines 15-23; shows a response of the receiver (port 24) to data packet received from

transmitter (entity 27) wherein the response involves a process by which the receiver updates the available credits and when possible, provides additional credits to the transmitter. The process takes place whenever port 24 receives a new packet. Also at col. 1, lines 40-45, Bloch shows that the receiver provides the transmitter with credit limits indicating the total amount of data that the transmitter has been authorized to send. The transmitter is not permitted to send anymore data if the credit limit has been exhausted (diminished).); storing the packet in a plurality of receiver buffers at the link receiver storing the packet in a receiver buffer at the link receiver (col. 3, lines 27-29; shows a step of receiving the data in the receive buffer responsive to the allocated credits.); transmitting the packet out of the receiver buffer at the link receiver on an egress link (col. 3, lines 30-31; shows the step of passing the data from the receive buffer for onward transmission through the network. At col. 8, lines 13-21, Figure 1; shows the method (figure 5 flowchart) is invoked whenever port 24 passes a packet from queue 28 to switching core 22 for onward transmission.); the free buffer pool corresponds to additional data credits (Based from the specification of the application (Wise) at Par. 0033, it shows that free buffer pool represents the empty portion of the receiver buffer. Therefore, the examiner interprets this limitation as resetting the receive buffer space that was used by the packet back to being an empty/unused part of the receive buffer. This interpretation is also applied to the remainder of the office action. Bloch shows at Figure 5, a flow chart that illustrates a method of reallocation of credits in receive queues 28 after a data packet has passed out of buffer 25. At col. 8, lines 22- 51, shows the different scenarios of credit (of buffer space) reallocation when

the packet was passed out of the buffer.). However, Bloch does not show the steps of allocating at the link transmitter a plurality of data credits to a plurality of logical channels; and placing the plurality of receiver buffers in a free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers, wherein the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed. Also, Bloch does not show a plurality of receive buffers.

Jones shows the step of allocating at the link transmitter the plurality of data credits to a plurality of logical channels (Figure 1, plurality of virtual channels, VC0-N; Figure 5; col. 2, lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify method of Bloch to include the selection of logical channels of Jones in order to bypass the need for an acknowledgement packet, resulting in reliable transmissions and efficient use of bandwidth (Jones, col. 2, lines 7-9). Jones does not show a plurality of receiver buffers and the step of placing the plurality of receiver buffers in a free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers, wherein the portion of the packet is proportional to a ratio of an egress link speed to an ingress link speed.

Takase shows the step of placing the plurality of receiver buffers in a free buffer pool after a portion of the packet has been transmitted out of the plurality of receiver buffers, (Figure 6C, col. 8, lines 15-19; shows that the input rate flows at a rate over the minimum guaranteed bandwidth (output rate). At col. 8, lines 1-14; Figure 6C, Takase shows that as long as the level of the leaky bucket repeatedly increases and decreases around the threshold as the lower limit, and the input packets are transferred to the

output line without causing excessive residence in the packet buffer.); and wherein the portion of the packet is proportional to a ratio of the egress link speed to the ingress link speed (col. 8, lines 1-3; shows that to the leaky bucket each time a packet is read out from the buffer (output queue), "water" of a volume proportional to the packet length is poured. The leaky bucket shown in Figures 6A-6E, shows the relationship between the input speed and the output place.). It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method of modified Bloch to include the features of Takase, in order to manage the amount of data to be transmitted and/or received in a device.

As to claims 14 and 15, these claims are rejected using the same reasoning used in the rejection of claims 4 and 5, respectively.

As to claim 17, Bloch shows a switch (Figure 1, Switch 22), comprising: a receiver buffer coupled to receive a packet from a link transmitter, wherein the packet is stored in the plurality of receiver buffers, and wherein the switch transmits the packet out of the receiver buffer (col. 5, lines 7-9; Figure 1; shows Port 24 (receiver) and entity 27 (transmitter) are configured to communicate over a plurality of logical links all of which are carried over physical link 29. At col. 2, lines 15-25, Bloch shows that the receiver has a buffer where it holds data packets that it has receive over the physical link before passing the packets through the switch to another of the ports for further transmission through the fabric and also, that the transmitter transmits packets over a

given logical link; Figures 1-2, 4-5); a free buffer pool (col. 6, lines 31-33; The buffer space remaining, over and above the static allocations, is held in a pool of spare credits for dynamic sharing among the virtual lanes.); and a link receiver flow control algorithm, wherein the link receiver flow control algorithm places the receiver buffer into the free buffer pool as the packet is transmitting out of the receiver buffer (Bloch shows at Figure 5, a flow chart that illustrates a method of reallocation of credits in receive queues 28 after a data packet has passed out of buffer 25. At col. 8, lines 22- 51, shows the different scenarios of credit (of buffer space) reallocation when the packet was passed out of the buffer.). However, Bloch does not show that the link transmitter allocates a plurality of data credits to a plurality of logical channels and a plurality of receiver buffers.

Jones shows that the link transmitter allocates a plurality of data credits to a plurality of logical channels (Figure 1, plurality of virtual channels, VC0-N; Figure 5; col. 2, lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify method of Bloch to include the selection of logical channels of Jones in order to bypass the need for an acknowledgement packet, resulting in reliable transmissions and efficient use of bandwidth (Jones, col. 2, lines 7-9). Jones does not show a plurality of receiver buffers.

Takase shows a plurality of packet buffers (Figure 2, Packet Buffer 20-1 to 20-n). It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method of modified Bloch to include the plurality of packet buffers

of Takase, as shown above, in order to increase the amount of data to be transmitted and/or received in a device.

As to claim 18, this claim is rejected using the same reasoning set forth in the rejection of claim 2. As to the additional claim limitations, the switch is coupled to receive the packet on an ingress link and coupled to transmit the packet on an egress link, refer to Figure 1 of Bloch.

As to claims 19, 20, 21, and 22, these claims are rejected using the same reasoning set forth in the rejection of claims 3, 4, 7 and 8, respectively.

As to claim 23, this claim is rejected using the same reasoning set forth in the rejection of claim 1. As to the additional claim limitation, a computer-readable medium encoded with computer executable instructions for instructing a processor to perform a method of early buffer return, refer to Bloch, col. 5, lines 2-4.

As to claims 24 and 25, these claims are rejected using the same reasoning set forth in the rejection of claims 3 and 5, respectively.

As to claim 27, this claim is rejected using the same reasoning set forth in the rejection of claim 13. As to the additional claim limitation, a computer-readable medium

encoded with computer executable instructions for instructing a processor to perform a method of early buffer return, refer to Bloch, col. 5, lines 2-4.

As to claims 28 and 29, these claims are rejected using the same reasoning set forth in the rejection of claims 14 and 15, respectively.

Response to Arguments

Applicant's arguments, see Applicant's Arguments/Remarks page 10-16, filed October 17, 2007, with respect to the rejection(s) of claim(s) 1, 7-9, 17, 21-23 under Bloch et al. (US 6922408) in view of Florin (US 6594701); claims 2-4, 10, 13-14, 18-20, 24, 27-28 under Bloch et al. (US 6922408) in view of Florin (US 6594701) in further view of Takase et al. (US 7023799); and claims 5-6, 11-12, and 25-26 under Bloch et al. (US 6922408) in view of Florin (US 6594701) in further view of Jones et al (US 6944173) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bloch et al. (US 6,922,408 B2) in view of Jones et al. (US 6944173 B1) in further view of Takase et al. (US 7023799 B2) for claims 1-5, 7-11, 13-15, 17-25, and 27-29.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Susnow et al. (US 7,190,667 B2) – note abstract;

Barkey et al. (US 5,825,748) – note abstract;

Bass et al. (US 7,072,299 B2) – note abstract;

Barrack et al. (US 6954424 B2) – note abstract.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Redentor M. Pasia whose telephone number is 571-272-9745. The examiner can normally be reached on M-F 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris H. To can be reached on (571)272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Redentor Pasia

DORIS H. TO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600